

# EE 330

## Lecture 3

- Integrated Circuit Design Flow
- Basic Concepts
  - Feature Sizes
  - Reliability

Review from last lecture:

# Moore's Law

(from Wikipedia)

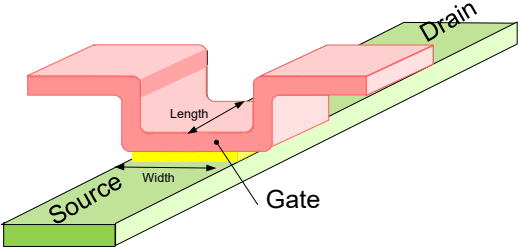
**Moore's law** is the empirical observation that the complexity of integrated circuits, with respect to minimum component cost, doubles every 24 months<sup>[1]</sup>. It is attributed to Gordon E. Moore<sup>[2]</sup>, a co-founder of Intel.

- Observation, not a physical law
- Often misinterpreted or generalized
- Many say it has been dead for several years
- Many say it will continue for a long while
- Not intended to be a long-term prophecy about trends in the semiconductor field
- Something a reporter can always comment about when they have nothing to say!

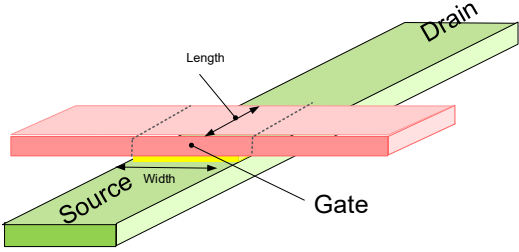
Device scaling, device count, circuit complexity, device cost, ... in leading-edge processes will continue to dramatically improve (probably nearly geometrically with a time constant of around 2 years ) for the foreseeable future !!

Review from last lecture:

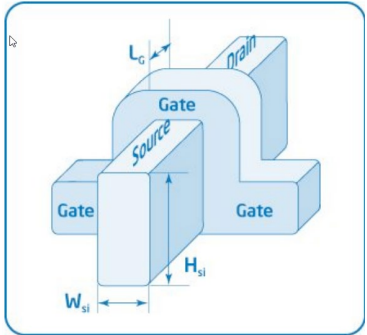
# Field Effect Transistors



Planar MOSFET (LOCOS)



Planar MOSFET (STI)

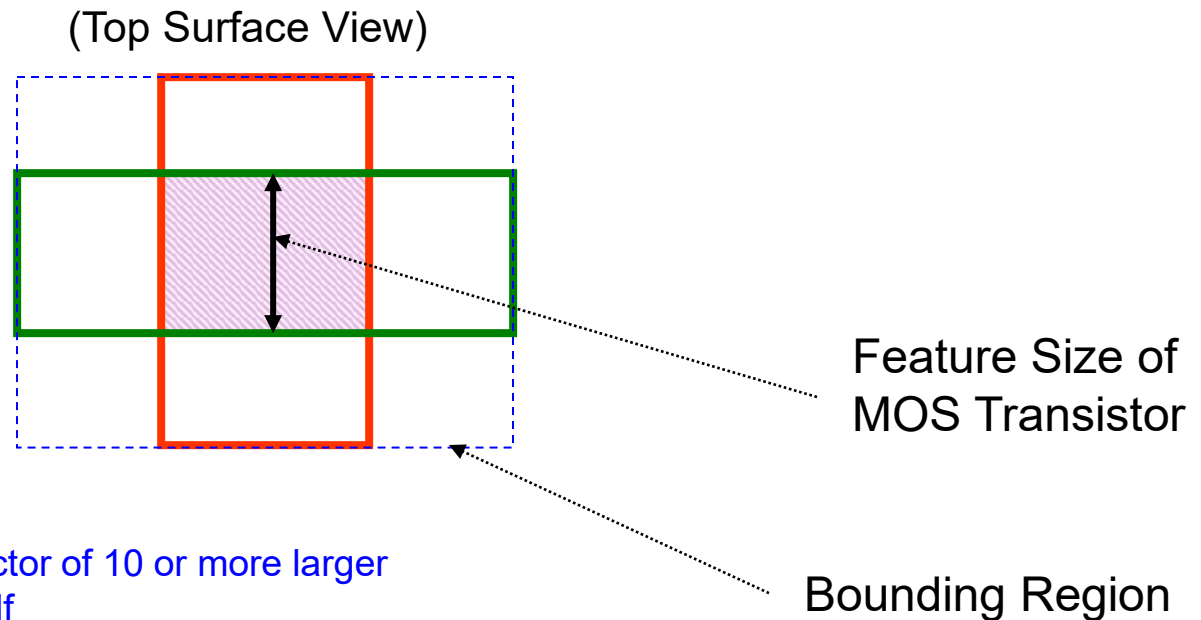


FinFET Tri-Gate  
Dielectric not shown

Review from last lecture:

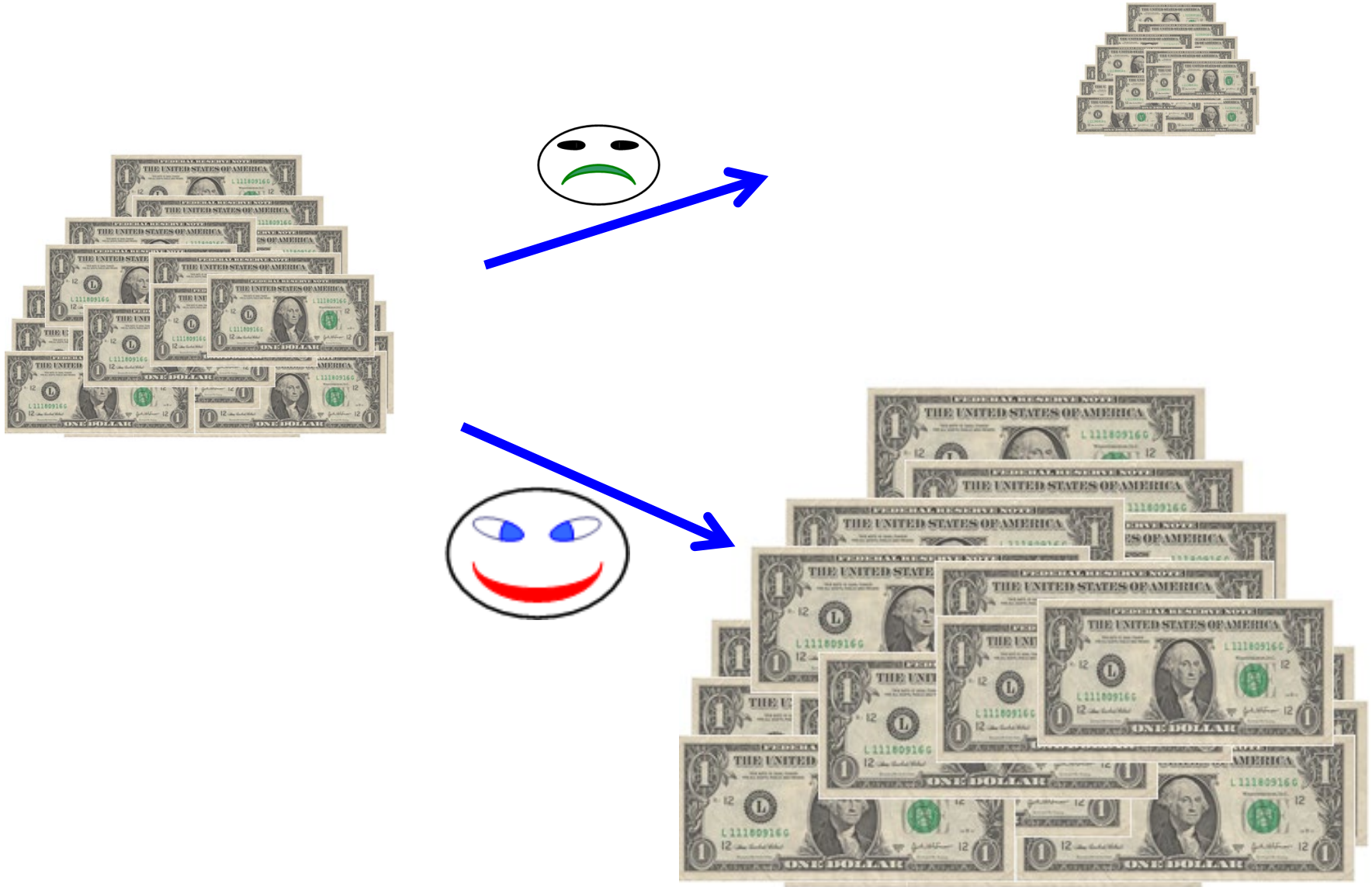
# Feature Size

The feature size of a process generally corresponds to the minimum lateral dimensions of the transistors that can be fabricated in the process



- Bounding region often a factor of 10 or more larger than area of transistor itself
- This along with interconnect requirements and sizing requirements throughout the circuit create an area overhead factor of 10x to 100x

# Review from last lecture: Considerable Cash Flow Inherent in the Semiconductor Industry



# Essentially All Activities Driven by Economic Considerations



- Many Designs Cost Tens of Millions of Dollars
- Mask Set and Production of New Circuit Approaching \$2 Million
- New Foundries Costs Approaching \$10 Billion (few players in World can compete)
- Many Companies Now Contract Fabrication (Fabless Semiconductor Companies)
- Time to Market is Usually Critical
- Single Design Error Often Causes Months of Delay and Requires New Mask Set
- Potential Rewards in Semiconductor Industry are Very High

**Will emphasize economic considerations throughout this course**

# Understanding of the Big Picture is Critical



# Solving Design Problems can be Challenging

Be sure to solve the right problem !





# How can complex circuits with a very large number of transistors be efficiently designed with low probability of error?

 Many designers often work on a single design

 Single error in reasoning, in circuit design, or in implementing circuit on silicon generally results in failure

- Design costs and fabrication costs for test circuits are very high
  - Design costs for even rather routine circuits often a few million dollars and some much more
  - Masks and processing for state of the art processes often between \$1M and \$2M
- Although much re-use is common on many designs, considerable new circuits that have never been designed or tested are often required
- Time to market critical – missing a deadline by even a week or two may kill the market potential

# Single Errors Usually Cause Circuit Failure

- How many components were typical of lab experiments in EE 201 and EE 230?
- Has anyone ever made an error in the laboratory of these courses ? (wrong circuit, incomplete understanding, wrong wiring, wrong component values, imprecise communication, frustration .....
- How many errors are made in a typical laboratory experiment in these courses?
- How many errors per hour might have occurred?

# Single Errors Usually Cause Circuit Failure

## **Consider an extremely complicated circuit**

- with requirements to do things that have never been done before
- with devices that are not completely understood
- that requires several billion transistors
- that requires 200 or more engineers working on a project full-time for 3 years
- with a company investment of many million dollars
- with an expectation that nobody makes a single error

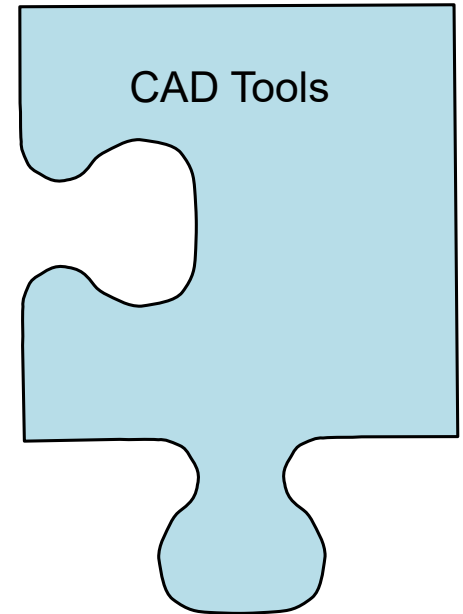
**Is this a challenging problem for all involved?**

# How can complex circuits with a very large number of transistors be efficiently designed with low probability of error?

- CAD tools and CAD-tool environment critical for success today
- Small number of VLSI CAD toolset vendors
- CAD toolset helps the engineer and it is highly unlikely the CAD tools will replace the design engineer
- An emphasis in this course is placed on using toolset to support the design process

# CAD Environment for Integrated Circuit Design

- Typical Tool Flow
  - (See Chapter 14 of Text)
- Laboratory Experiments in Course





# VLSI Design Flow Summary

Analog Flow

System Description

Circuit Design (Schematic)

Schematic Editor

SPICE Simulation

Spectre (or HSPICE)

Simulation Results  
Desired Results

Layout/DRC...

Assura DRC

LVS

Assura LVS

LVS Error Report

Assura RCX

Parasitic Extraction

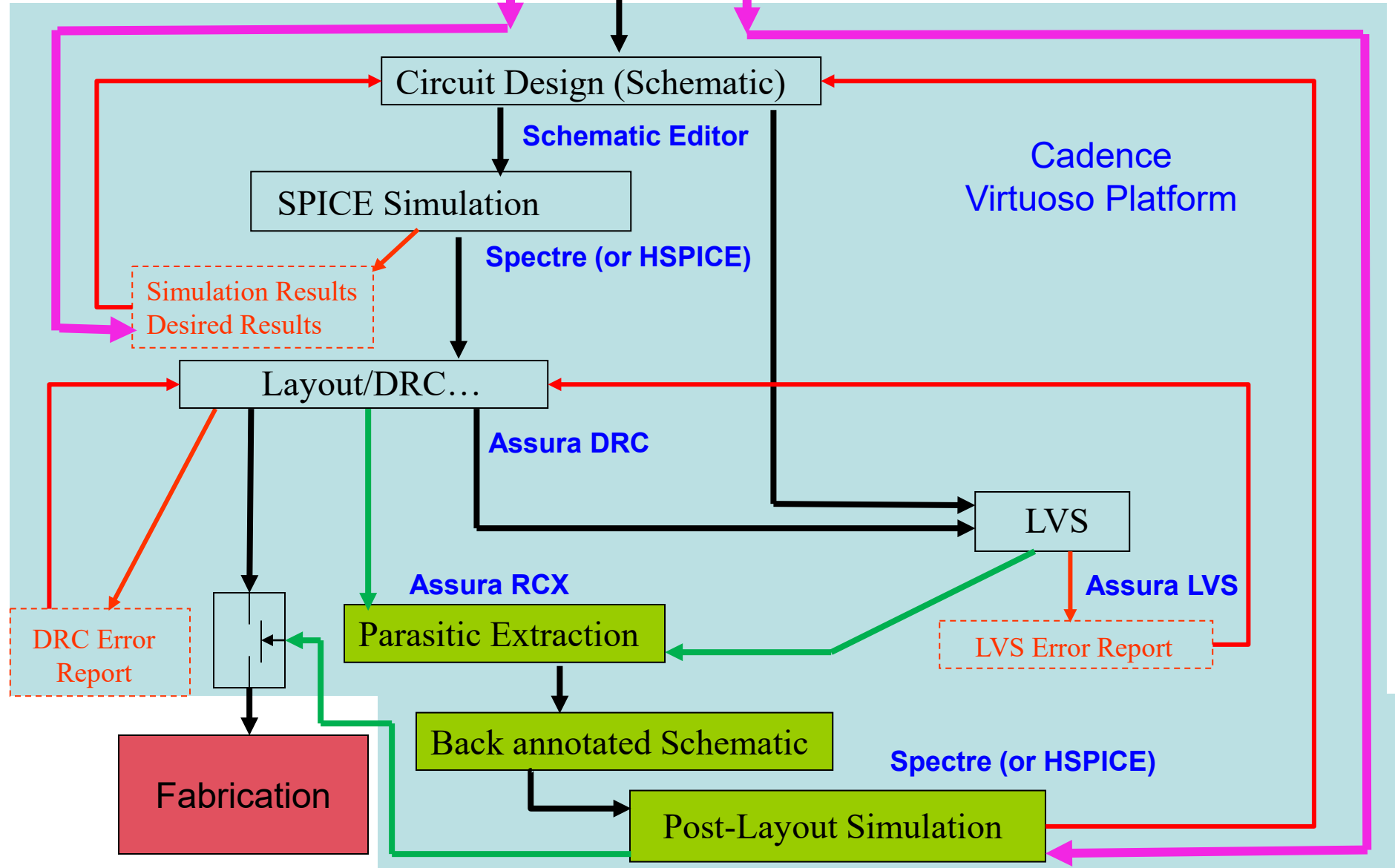
Back annotated Schematic

Spectre (or HSPICE)

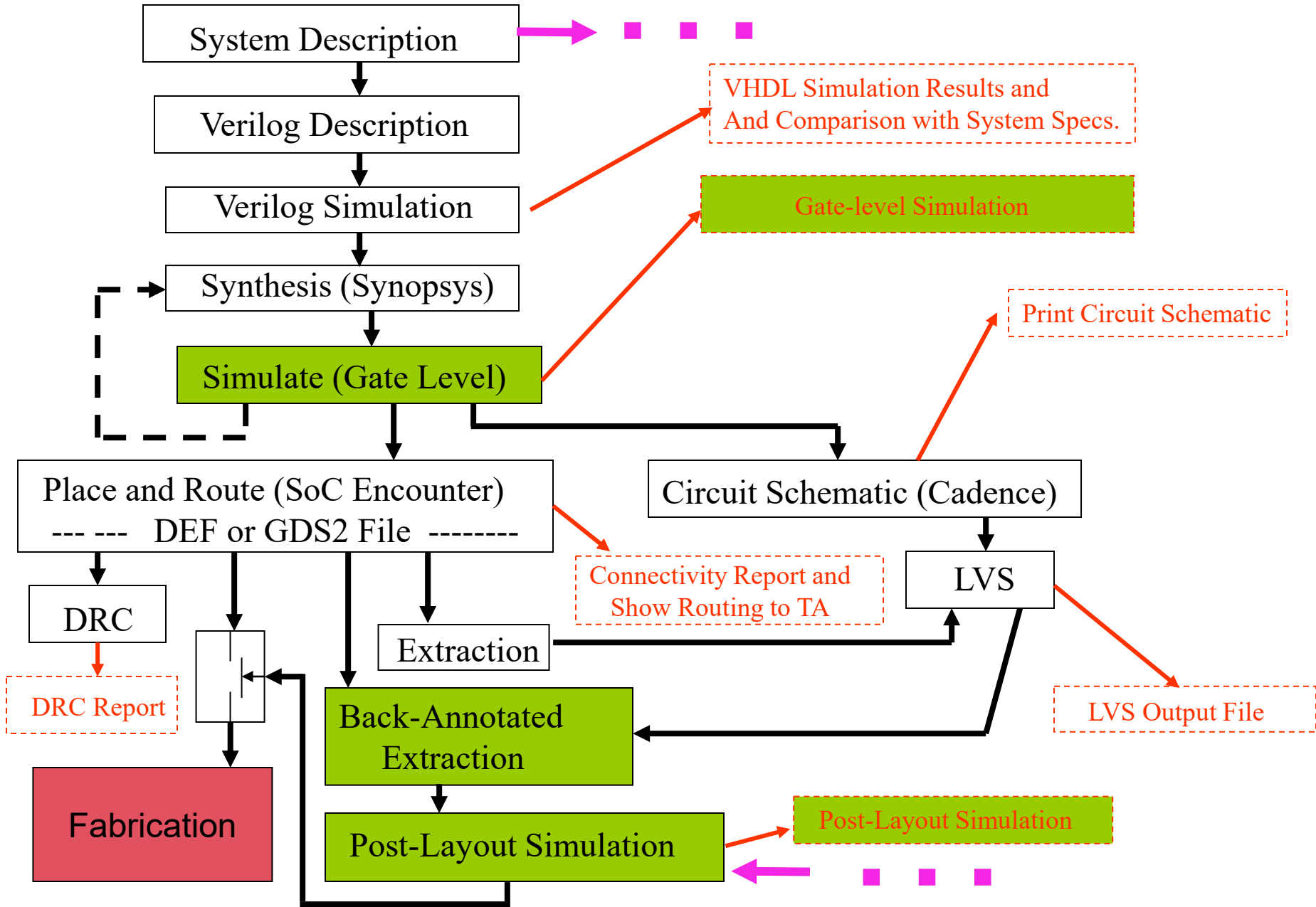
Post-Layout Simulation

Fabrication

Cadence  
Virtuoso Platform



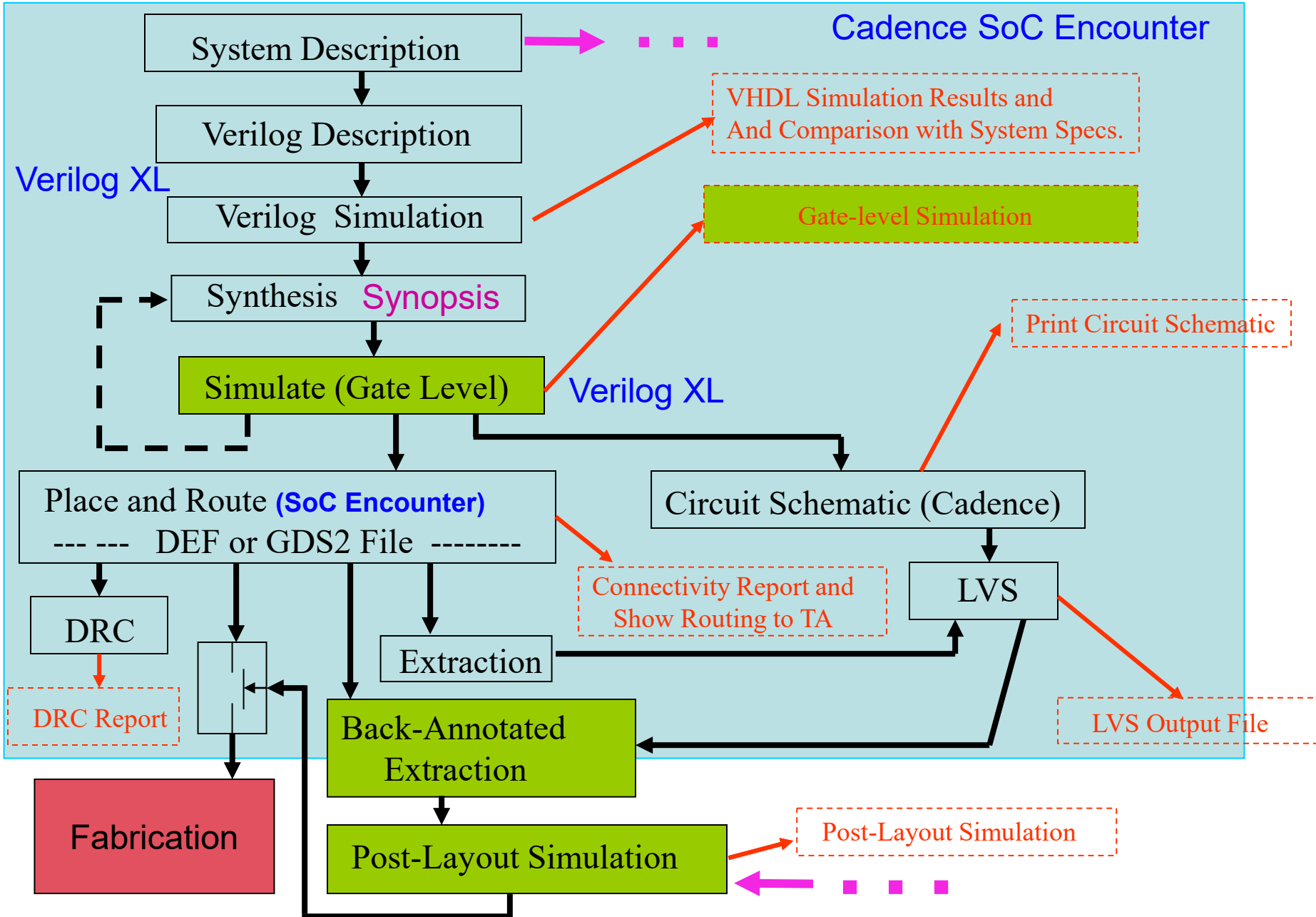
# VLSI Design Flow Summary





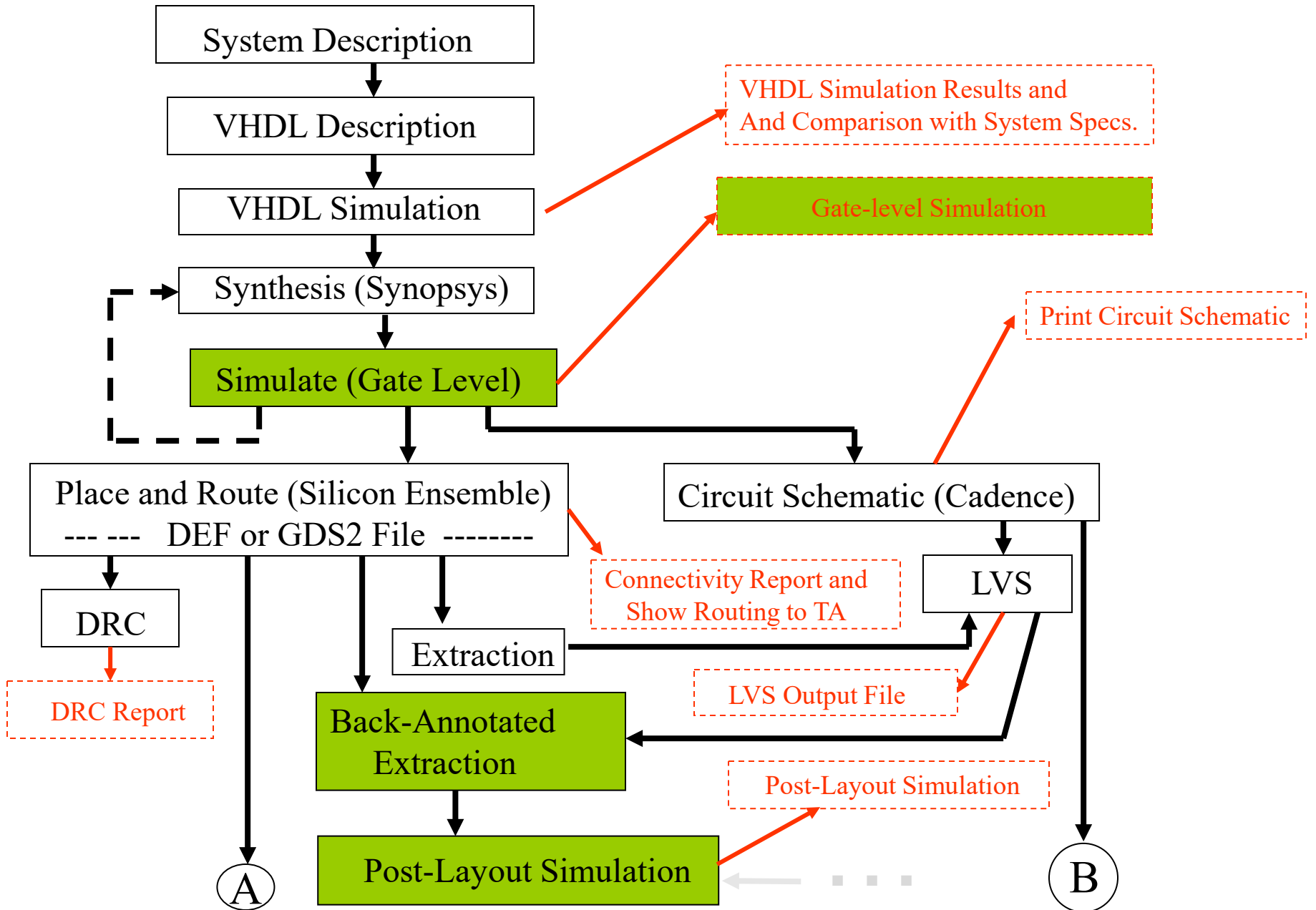
# VLSI Design Flow Summary

Digital Flow



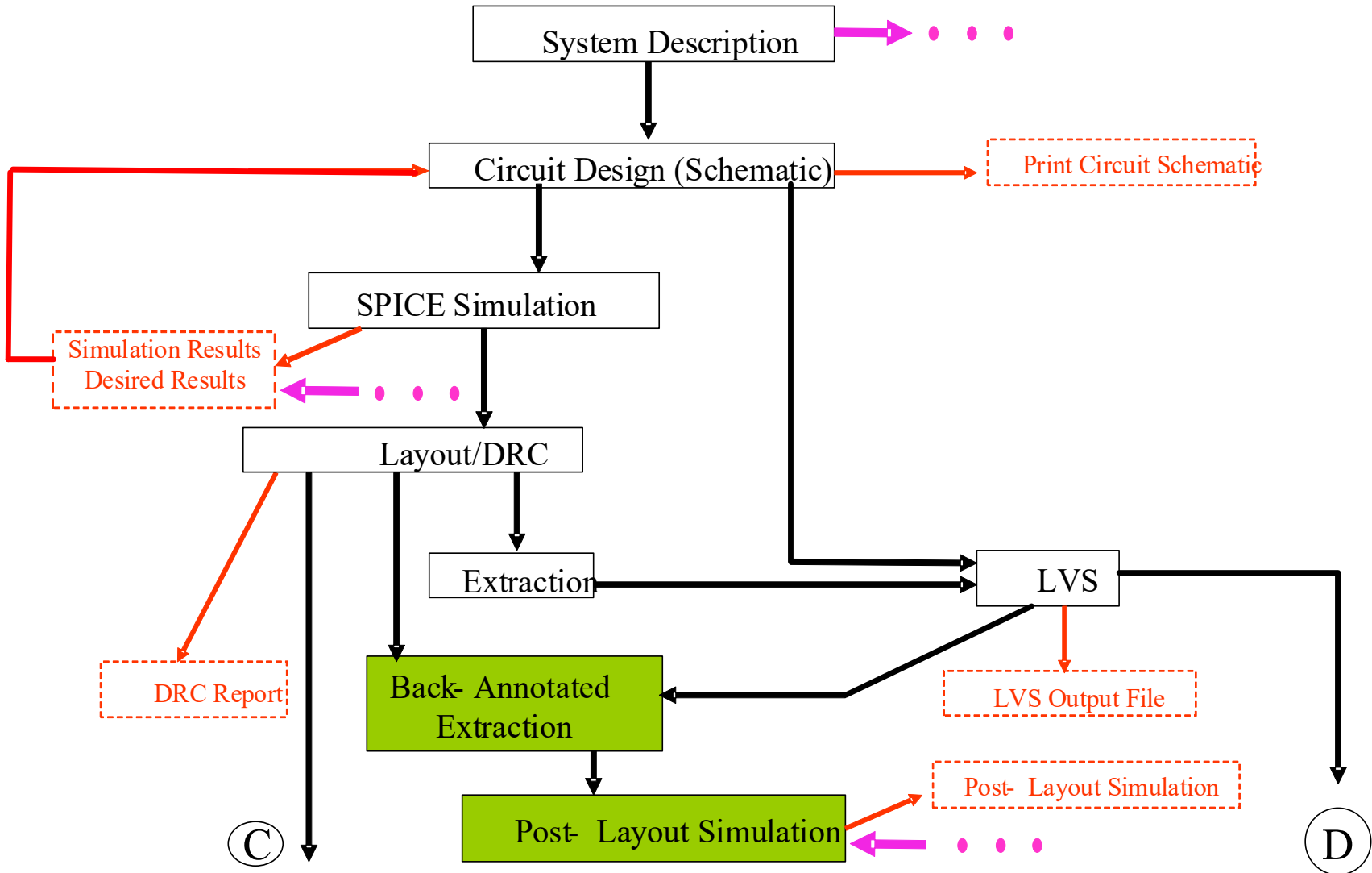
# VLSI Design Flow Summary

## Mixed Signal Flow (Digital Part)



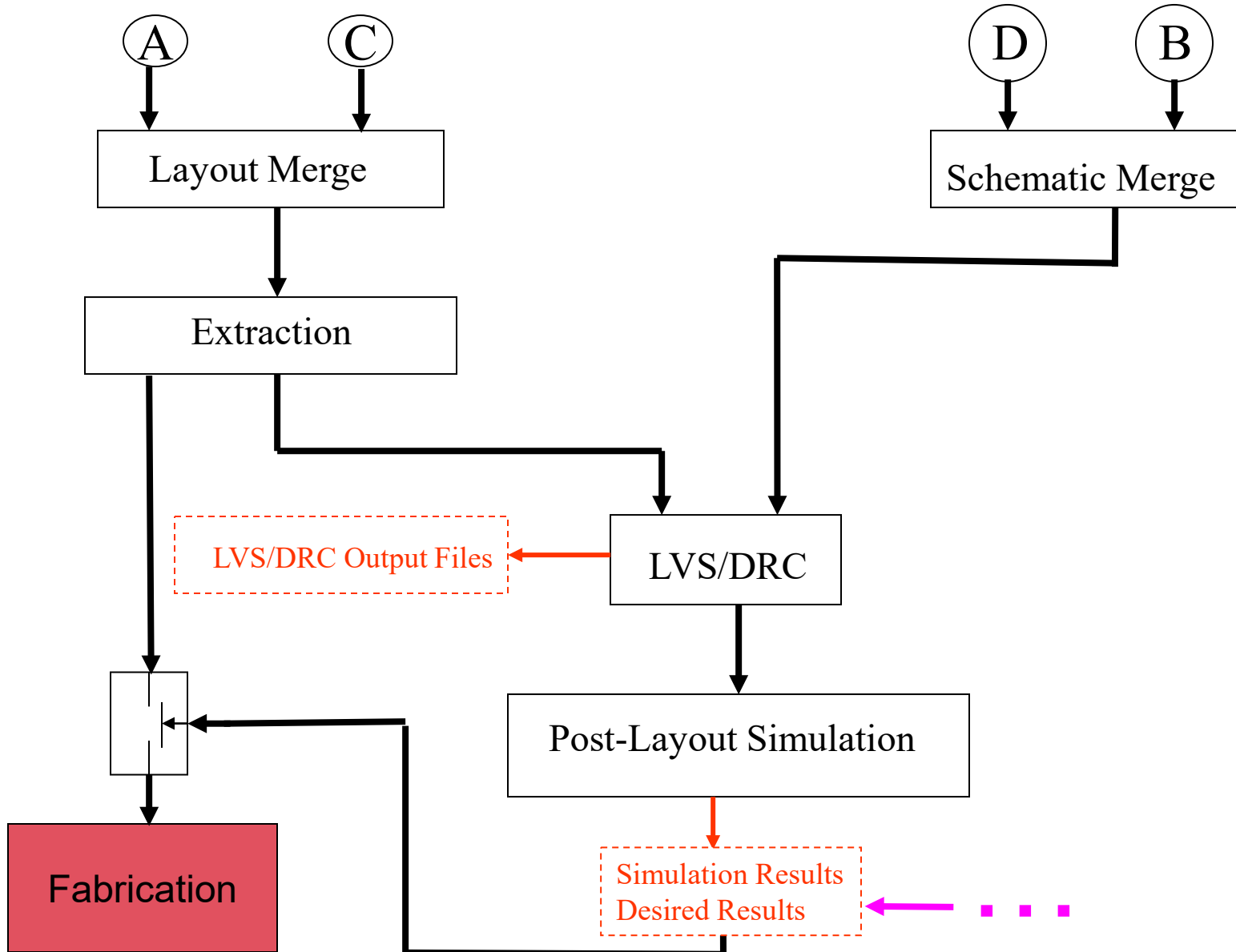
# VLSI Design Flow Summary

## Mixed - Signal Flow (Analog Part)



# VLSI Design Flow Summary

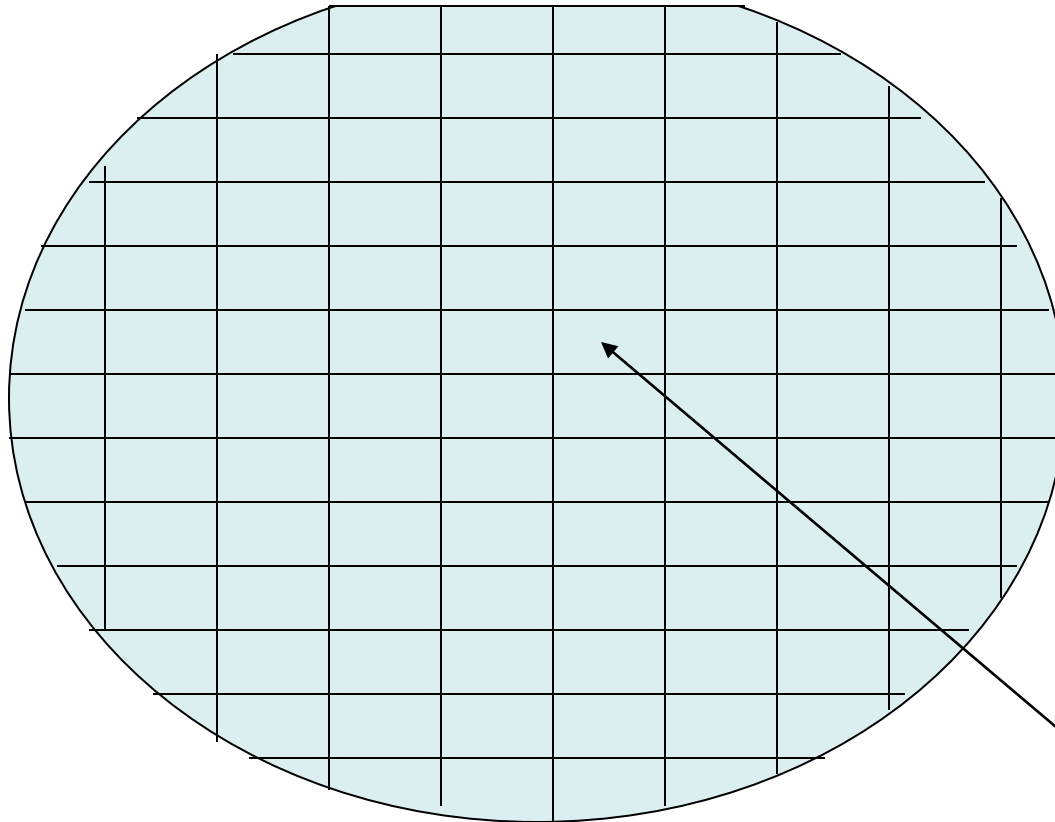
## Mixed-Signal Flow (Analog-Digital Merger)



# Comments

- The Analog Design Flow is often used for small digital blocks or when particular structure or logic styles are used in digital systems
- Variants of these flows are widely used and often personalized by a given company or for specific classes of circuits

# Wafer

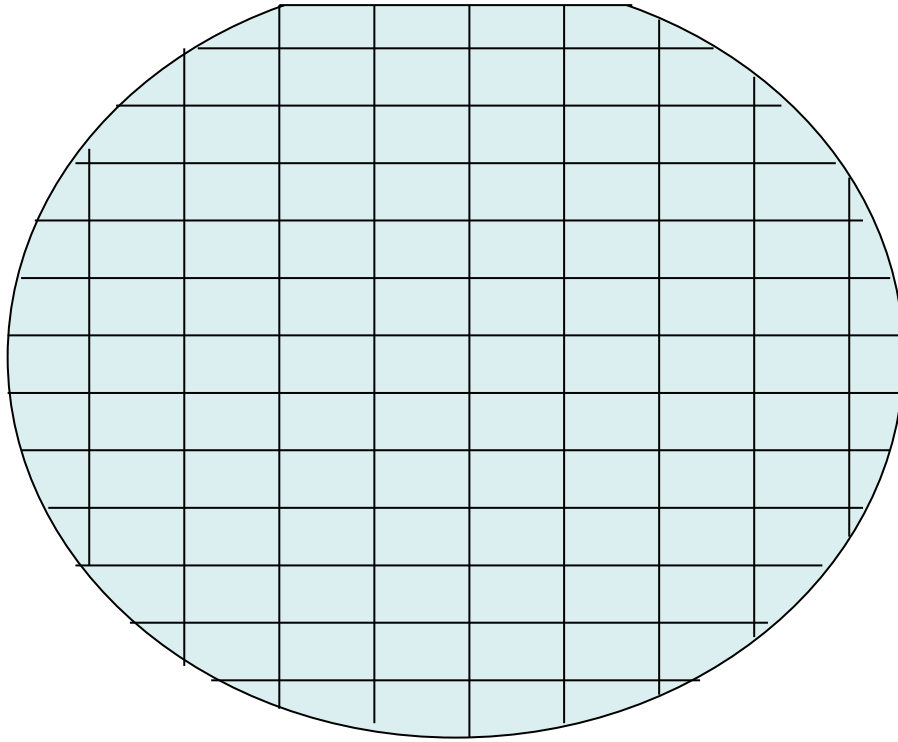


- 6 inches to 18 inches in diameter
- All complete cells ideally identical
- flat edge
- very large number of die if die size is small



die

# Why are wafers round?



- Ingot spins (rotates) as crystal is being made (dominant reason)
- Edge loss would be larger with rectangular wafers
- Heat is more uniformly distributed during processing
- Size of furnace is smaller for round wafers
- Wafers are spun during application of photoresist and even coatings is critical
- Optics for projection are better near center of image

# Feature Size

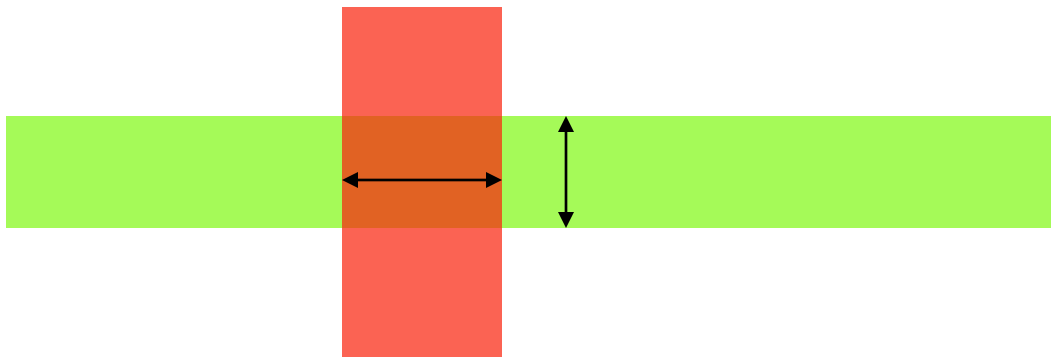
Feature size is the minimum lateral feature size that can be **reliably** manufactured



Often given as either feature size or pitch

Minimum feature size often identical for different features

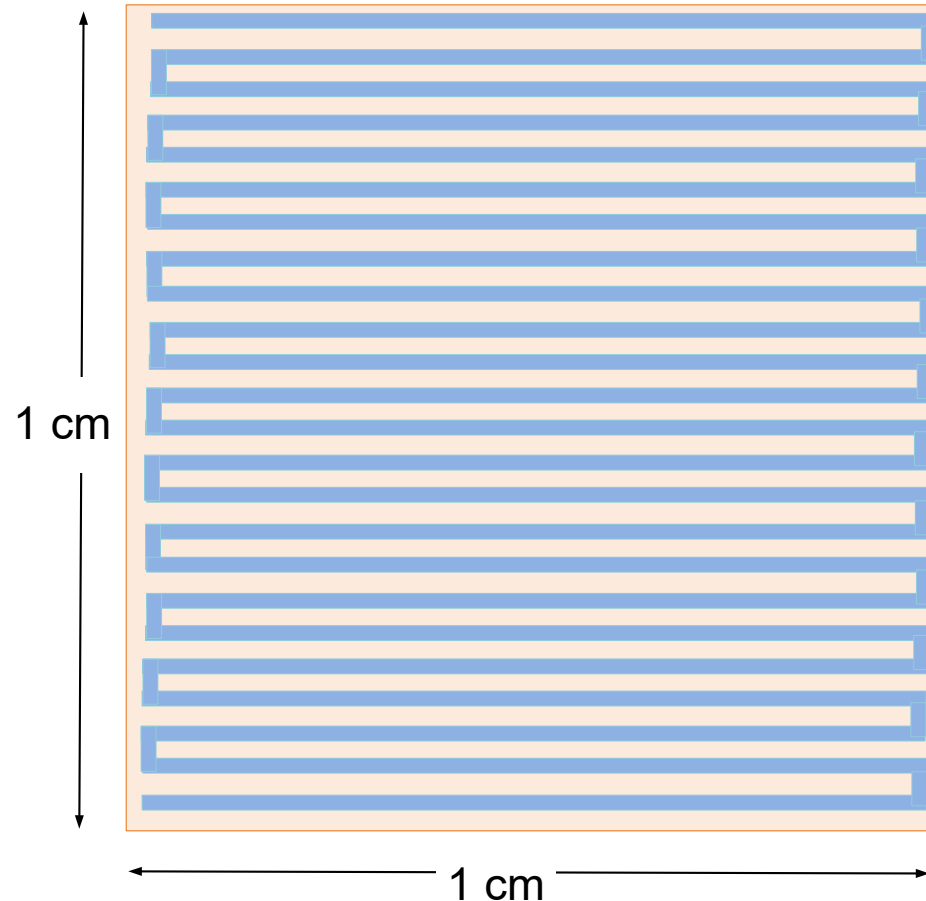
Extremely challenging to decrease minimum feature size in a new process





# Reliability

Consider the following example:



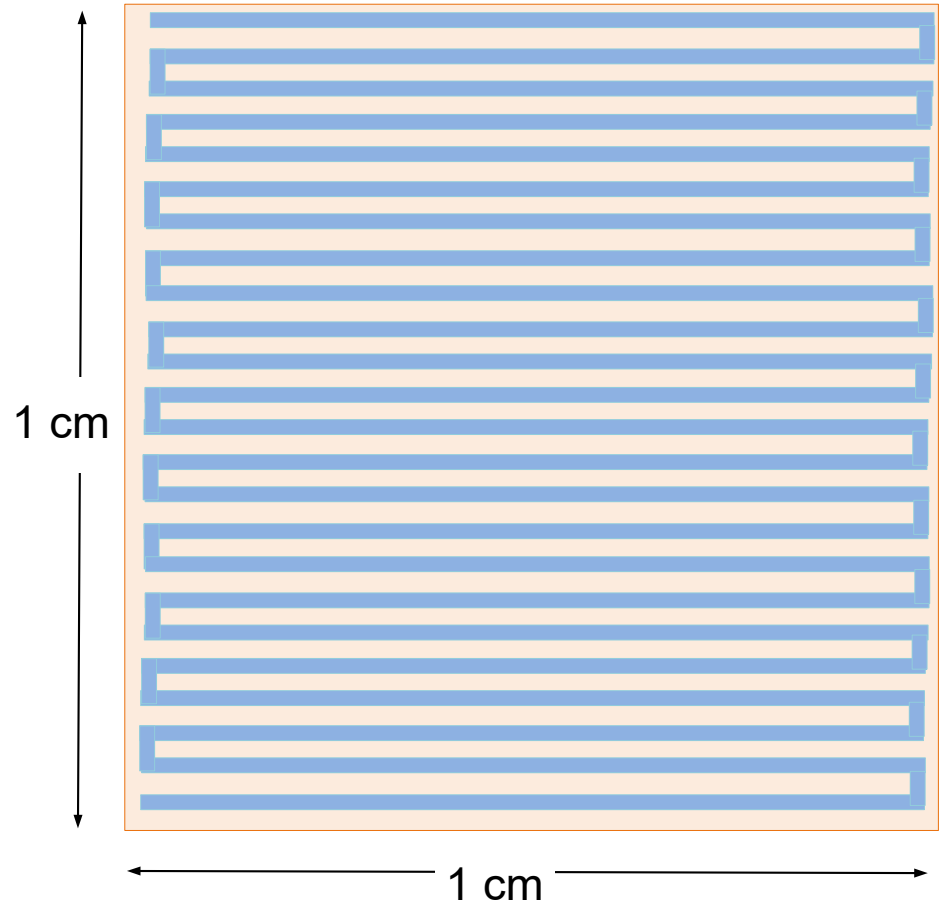
Assume:

- Die contains only interconnect
- Area  $1\text{cm}^2$
- 5nm process (10nm pitch)
- 10 levels of interconnect (actually pitch will increase in higher levels but ignore that)

**How long is the total interconnect?**

# Reliability

How long is the total interconnect?



$n$  = number of stripes:

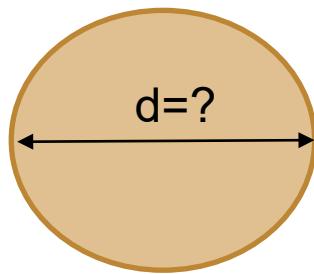
$$n = \frac{1\text{cm}}{5\text{nm} + 5\text{nm}} = \frac{10^{-2}}{10 \times 10^{-9}} = 10^6$$

$$L = n_{\text{LEVELS}} \cdot L_{\text{LEVEL}} = 10 \cdot 10^6 \times 1\text{cm} = 100\text{km}$$

$$L = 62 \text{ miles}$$

# Reliability

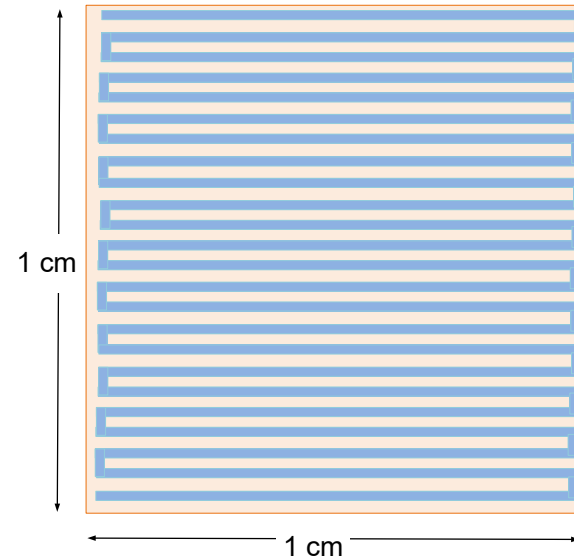
In perspective:



Human Hair



5nm



How do these dimensions compare to that of the human hair?

Human Hair Diameter: 18 $\mu$ m to 180 $\mu$ m

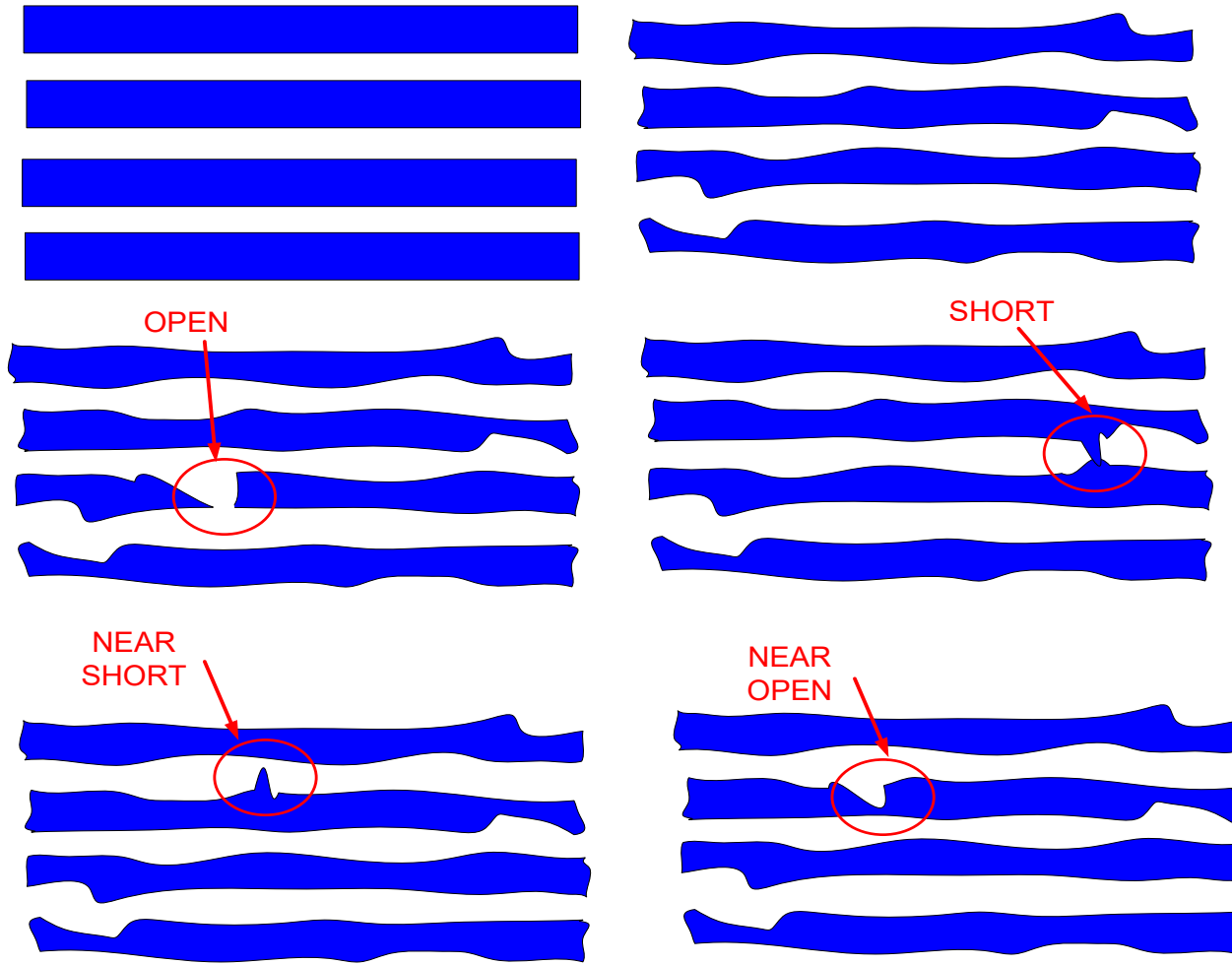
Assume d=50 $\mu$ m

$$r = \frac{d}{5\text{nm}} = \frac{50\mu\text{m}}{5\text{nm}} = 10,000$$

- Length of 5nm transistor 10,000 times smaller than the diameter of a 50 $\mu$ m hair
- If interconnect were square (not quite) cross-sectional area would be 100 million times smaller !

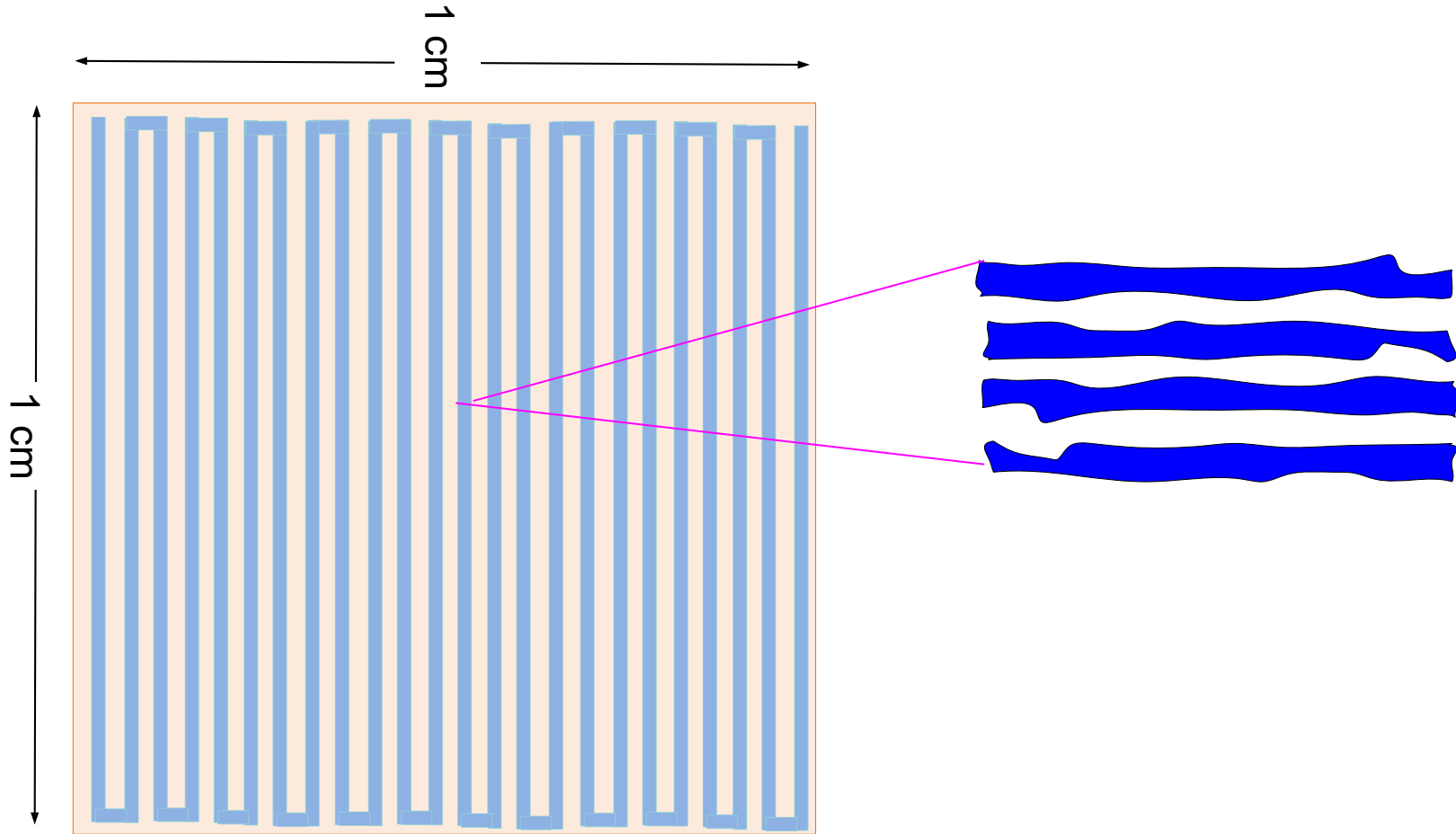
# Reliability Problems

## Desired Features



Actual features show some variability (dramatically exaggerated here !!!!)

# Reliability Challenges



Can not tolerate one defect in 62 miles in these interconnects that are 5nm wide

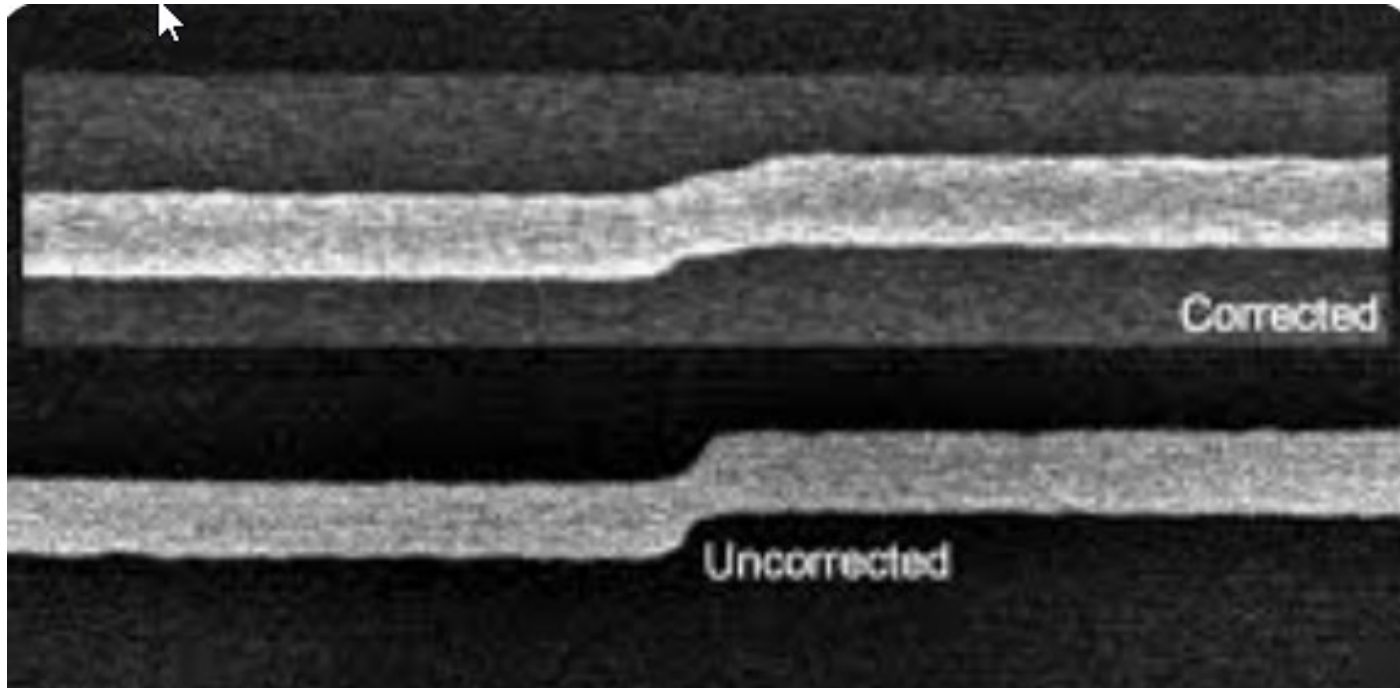
# Feature Size

Feature size is the minimum lateral feature size that can be **reliably** manufactured

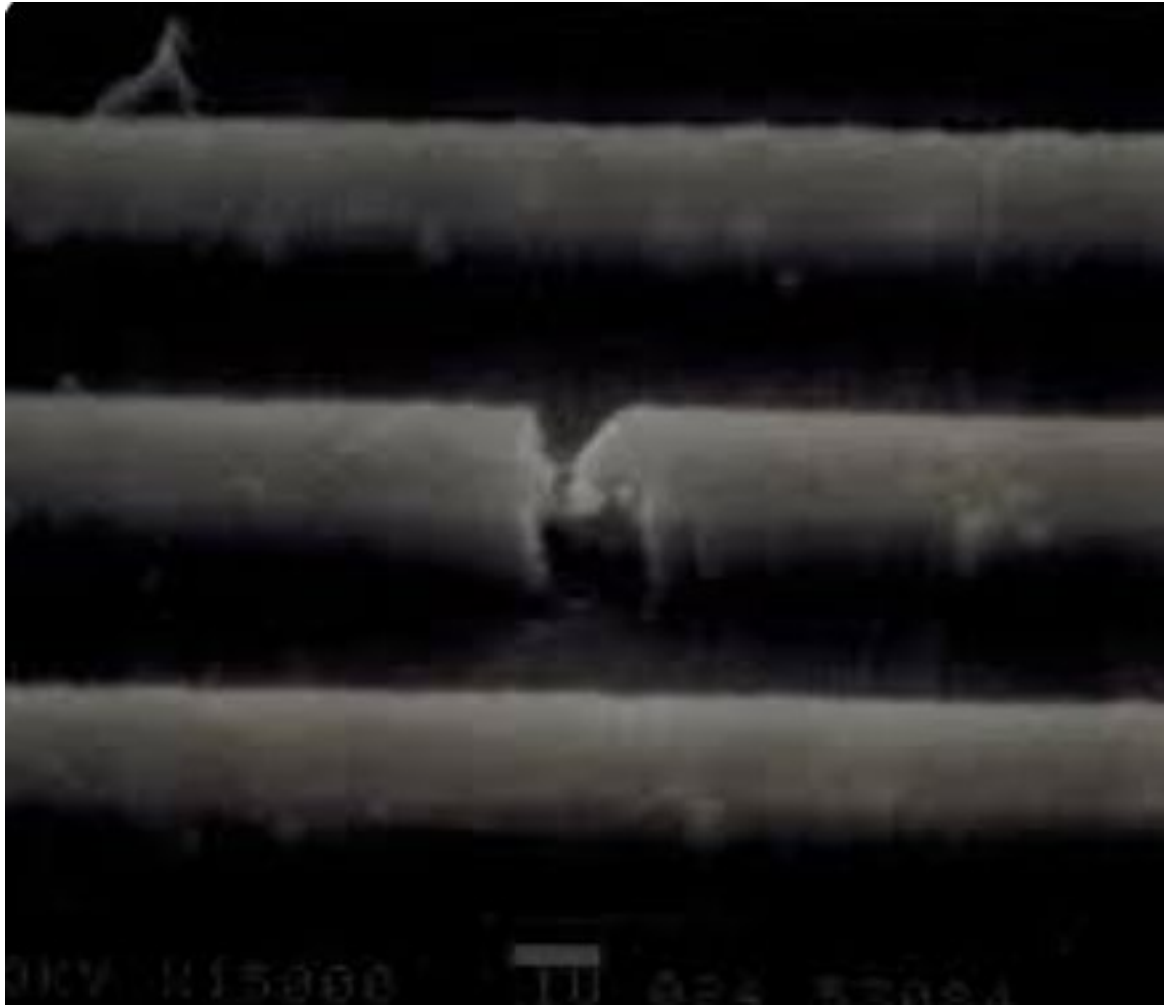


Feature size is specified so that there is a very low probability of a single processing defect occurring any place on a die !

# SEM Images of Irregularity and/or Defects

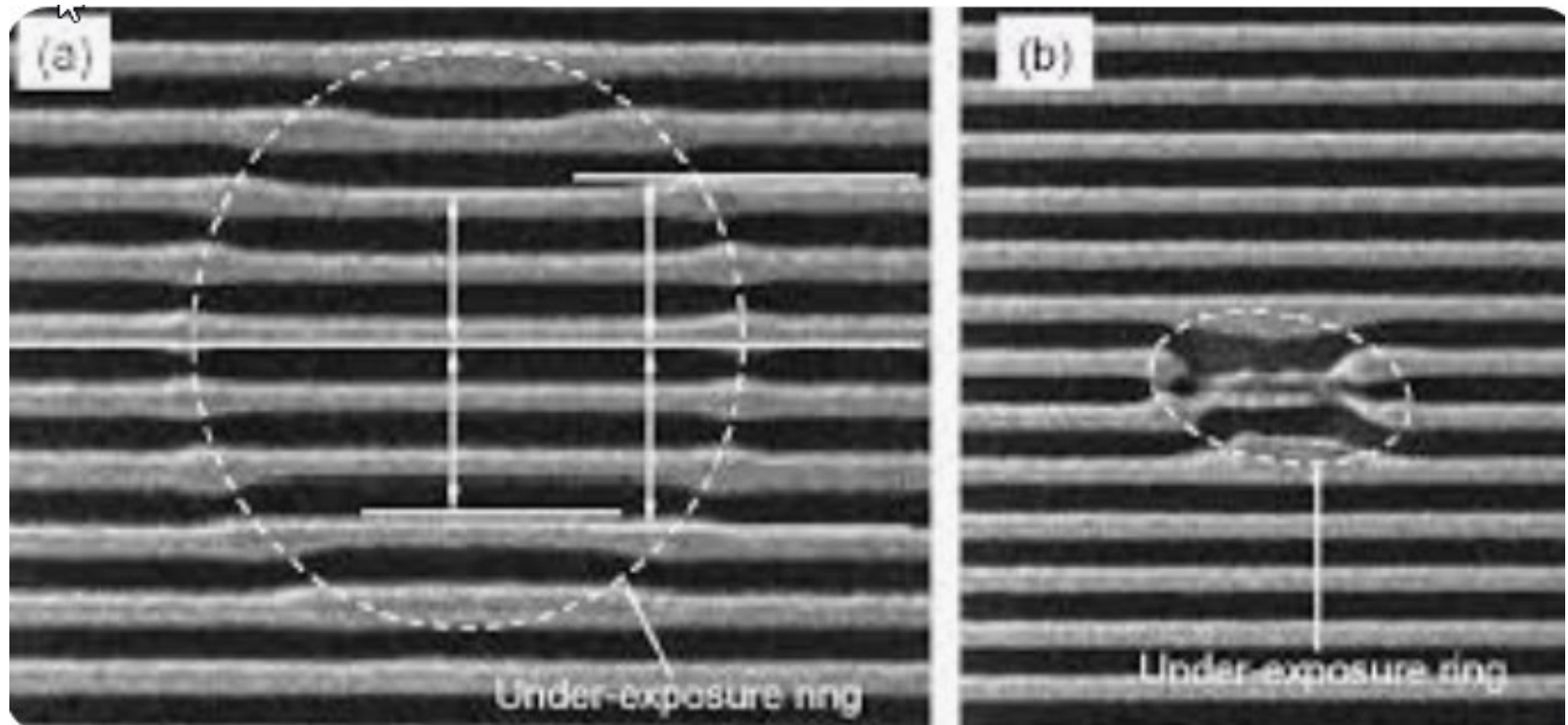


# SEM Images of Irregularity and/or Defects

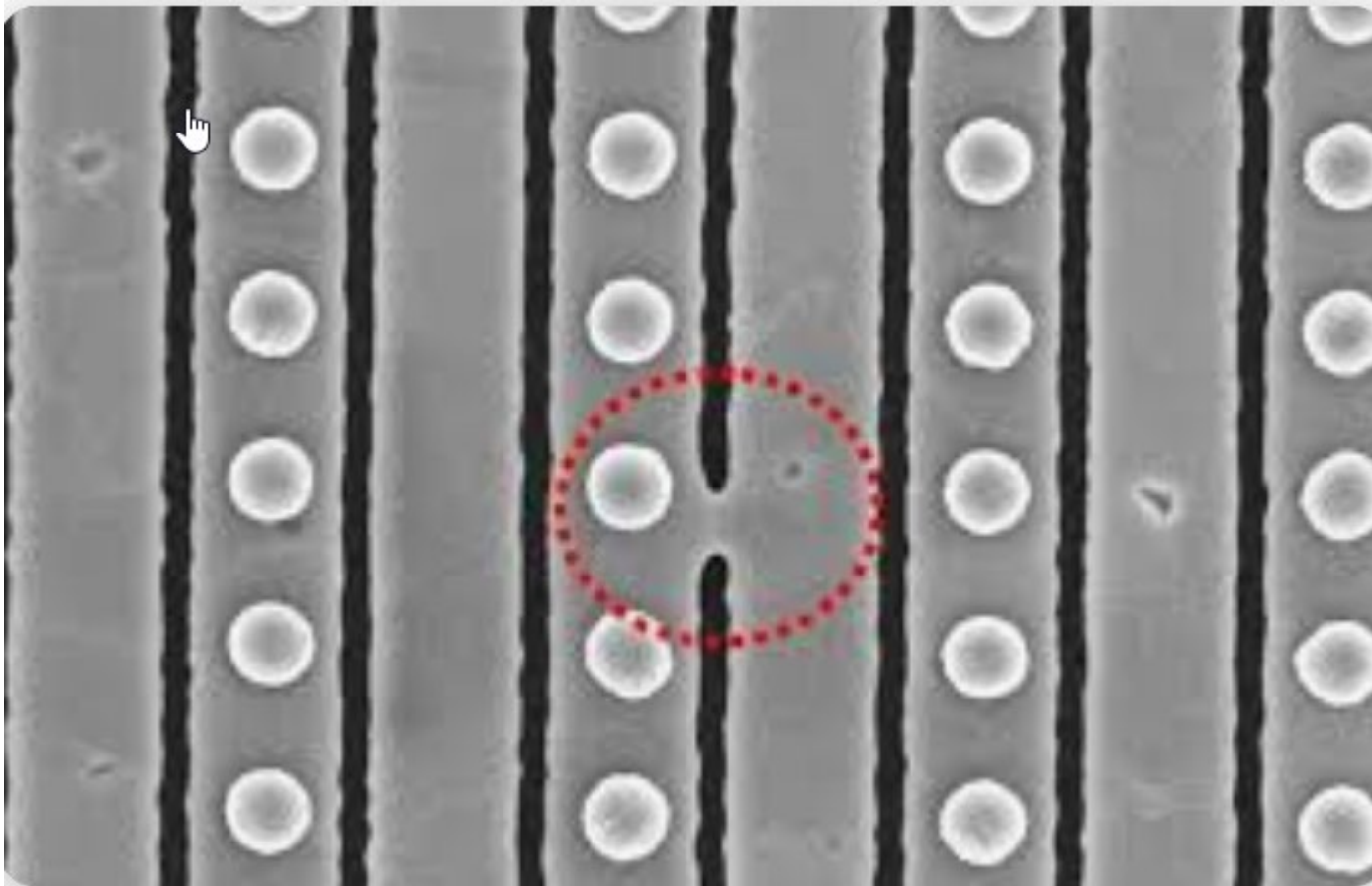




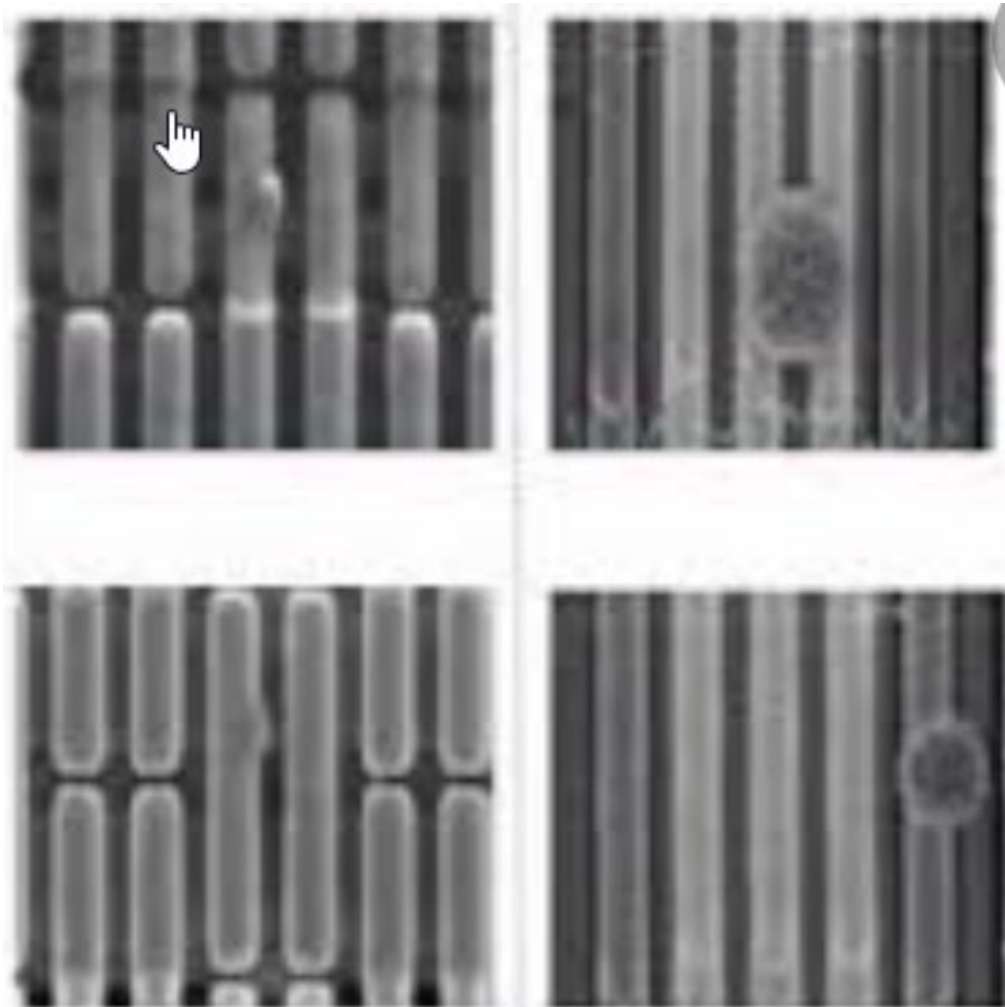
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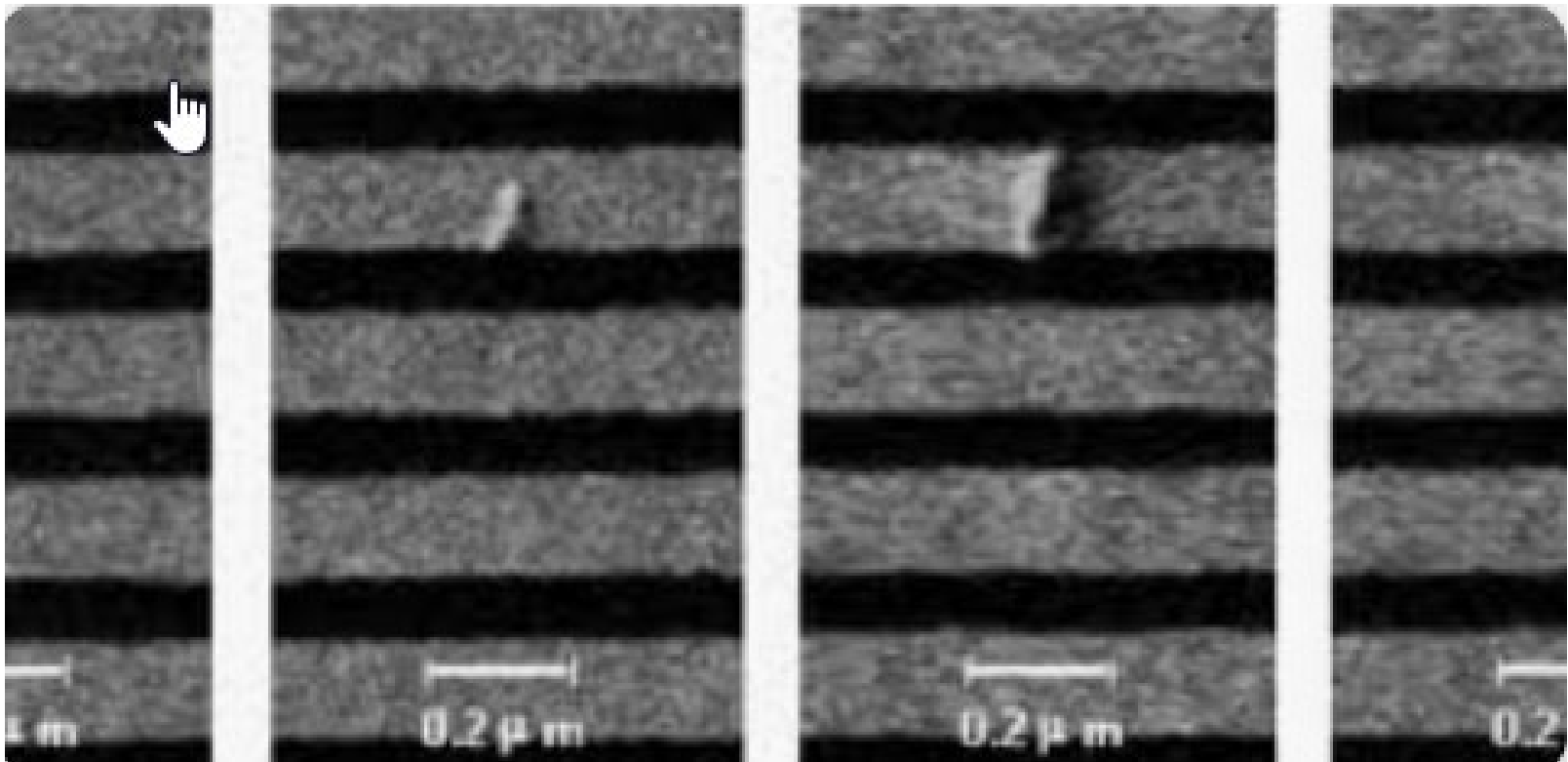
# SEM Images of Irregularity and/or Defects



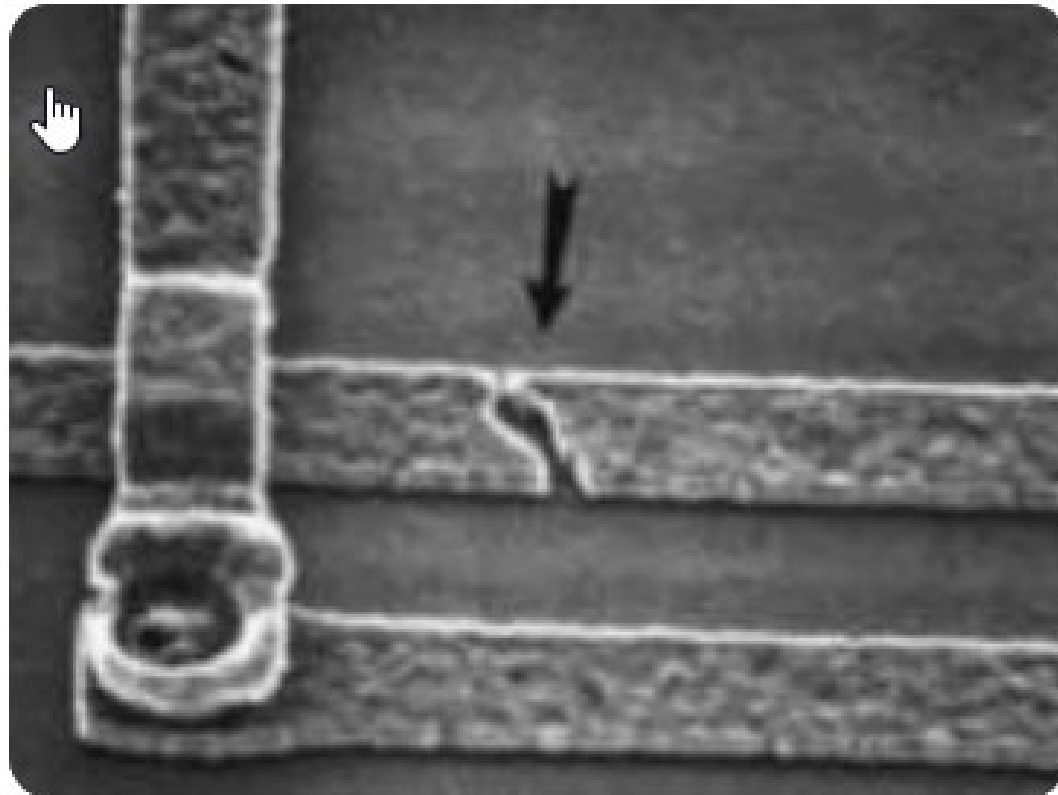
# SEM Images of Irregularity and/or Defects



# SEM Images of Irregularity and/or Defects



# SEM Images of Irregularity and/or Defects



Semiconductor Electromigration In...

# What is meant by “reliably”

Yield is acceptable if circuit performs as designed even when a very large number of these features are made

If  $P$  is the probability that a feature is good

$n$  is the number of uncorrelated features on an IC

$Y$  is the yield

$$Y = P^n$$

$$P = e^{\frac{\log_e Y}{n}}$$

# Example: How reliable must a feature be?

$$n=5E3$$

$$Y=0.9$$

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E3}} = 0.999979$$

But is  $n=5000$  large enough?                      is  $Y$  large enough?

More realistically  $n=5E9$  (or even  $5E10$ )

Consider  $n=5E9$

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E9}} = 0.999999999979$$

20 parts in a trillion or size of a piece of sheetrock relative to area of Iowa

**Extremely high reliability must be achieved in all processing steps to obtain acceptable yields in state of the art processes**

# Feature Size

- Typically minimum length of a transistor
- Often also minimum width or spacing of a metal interconnect (wire)
- Point of “bragging” by foundries
  - Drawn length and actual length differ
- Often specified in terms of pitch
  - Pitch is sum of feature size and spacing of same feature
  - Pitch approximately equal to twice minimum feature size



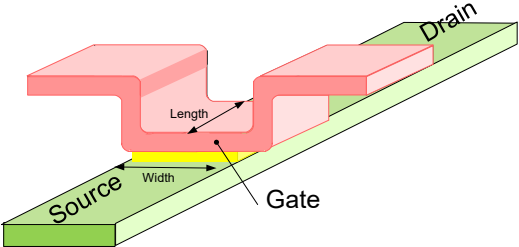
# Feature Size Evolution

Mid 70's	25 $\mu$
2005	90nm
2010	20nm
2020	7nm

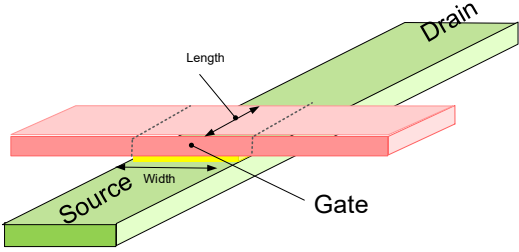
$$1\mu = 10^3 \text{ nm} = 10^{-6} \text{ m} = 10^4 \text{ \AA}$$

Review from last lecture:

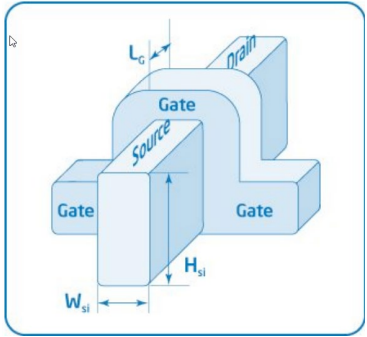
# Field Effect Transistors



Planar MOSFET (LOCOS)

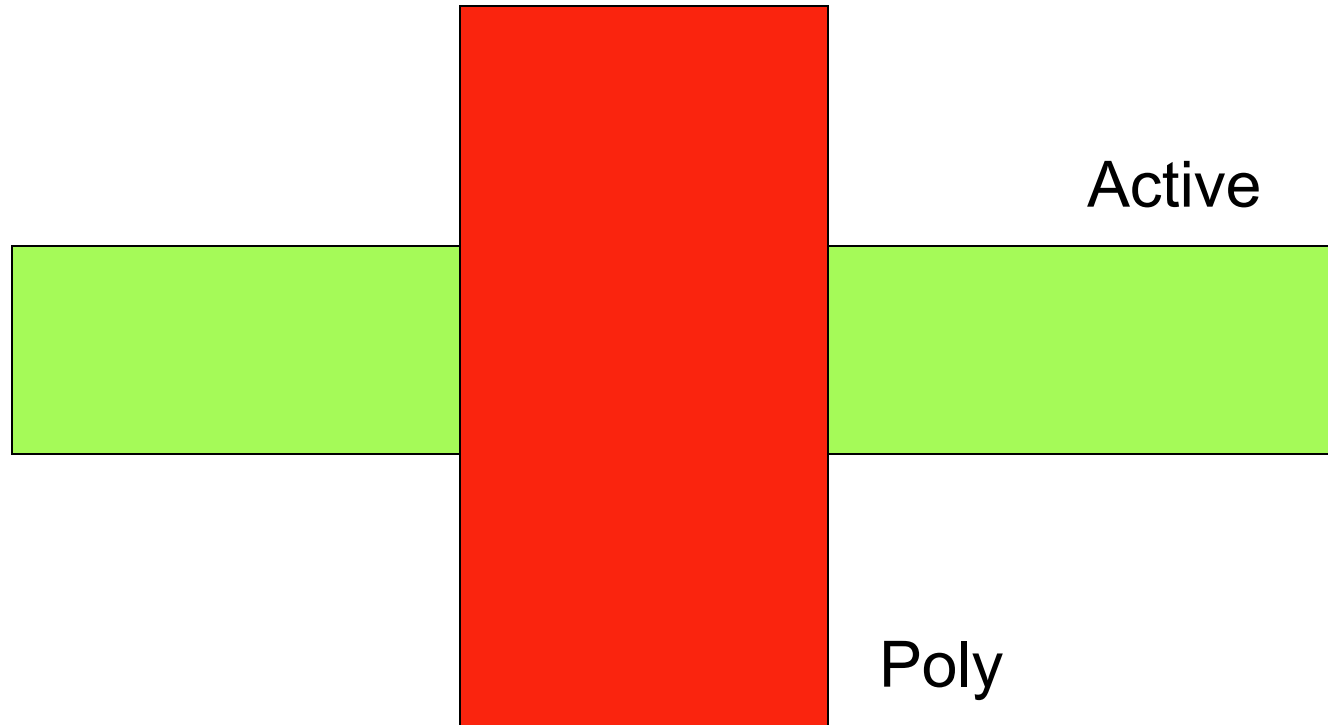


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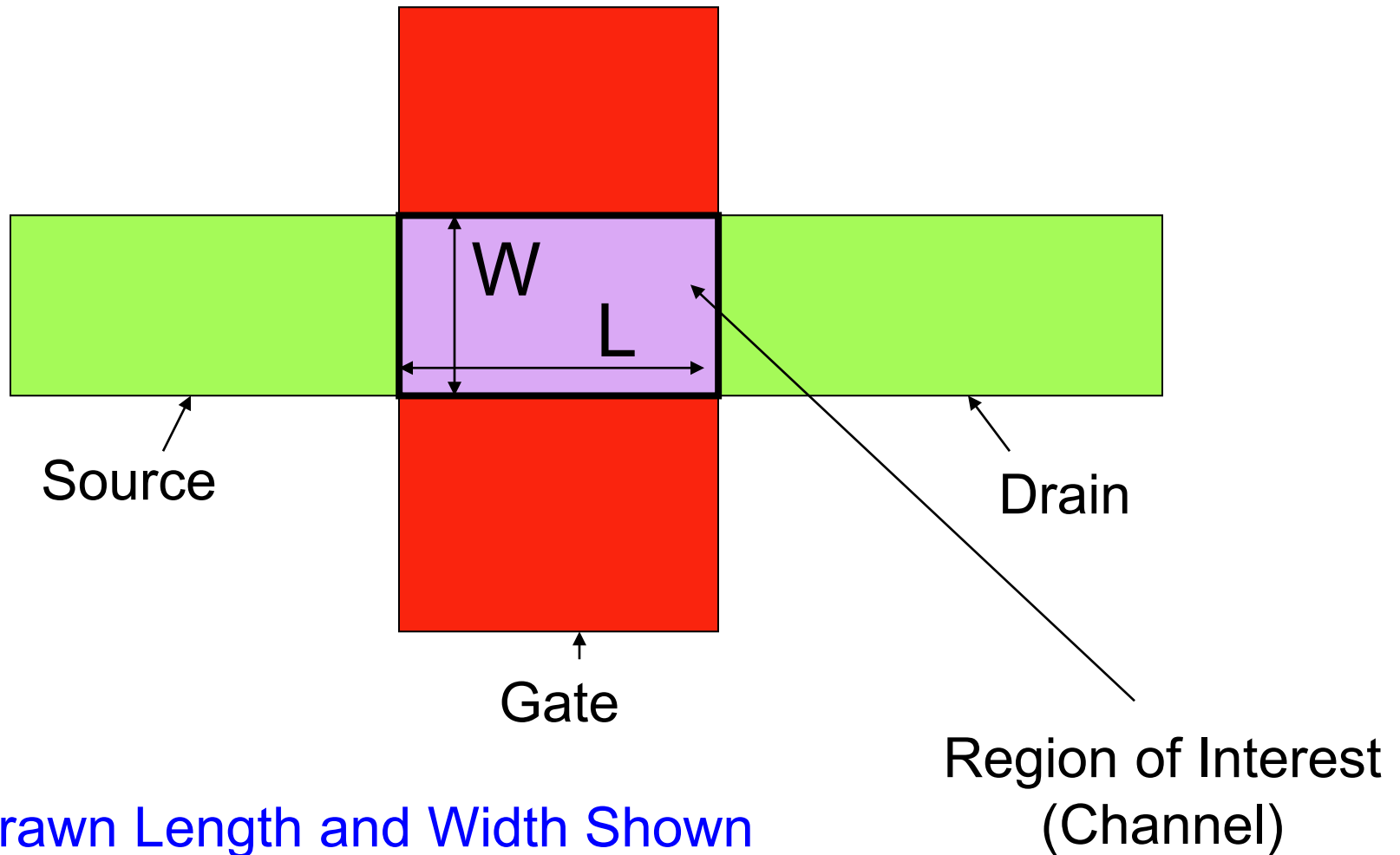


FinFET Tri-Gate  
Dielectric not shown

# Planar MOS Transistor

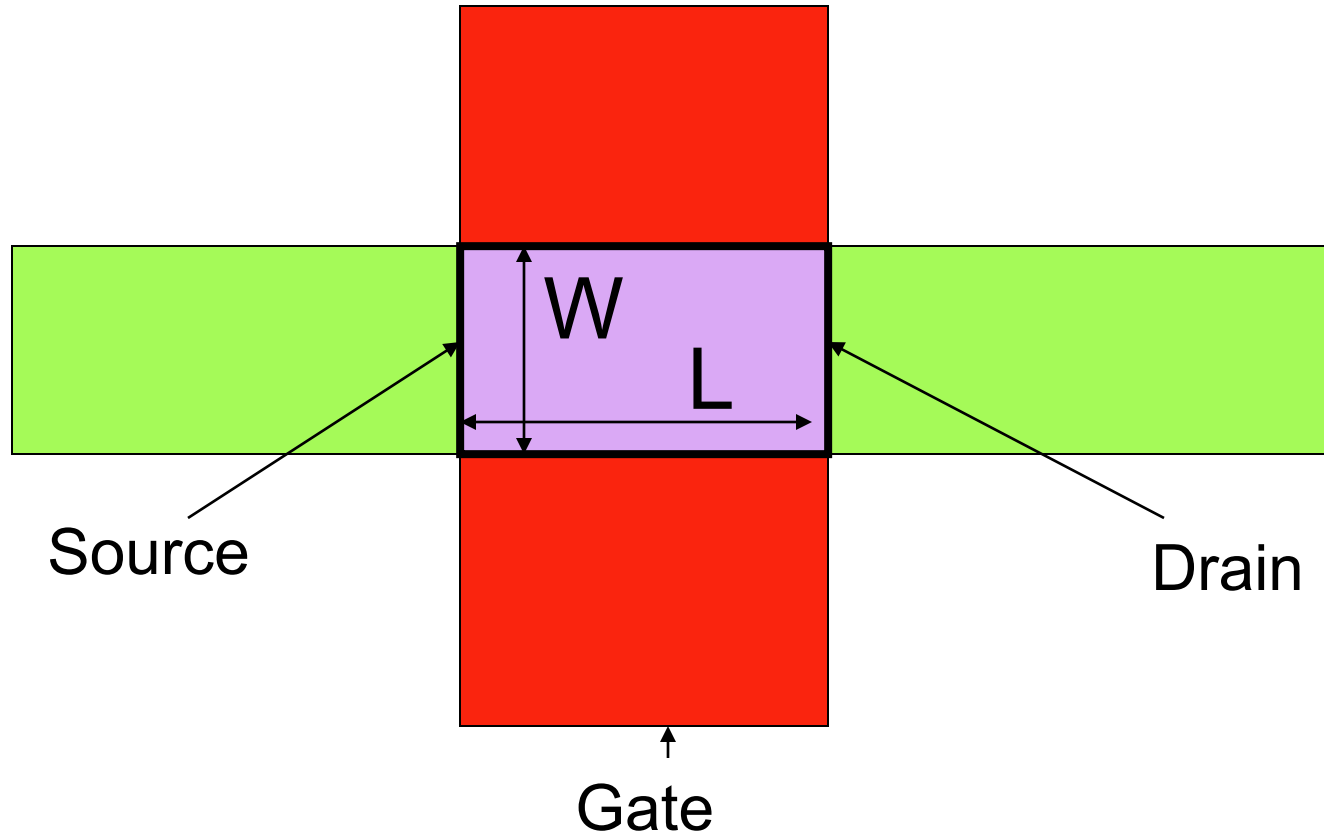


# Planar MOS Transistor



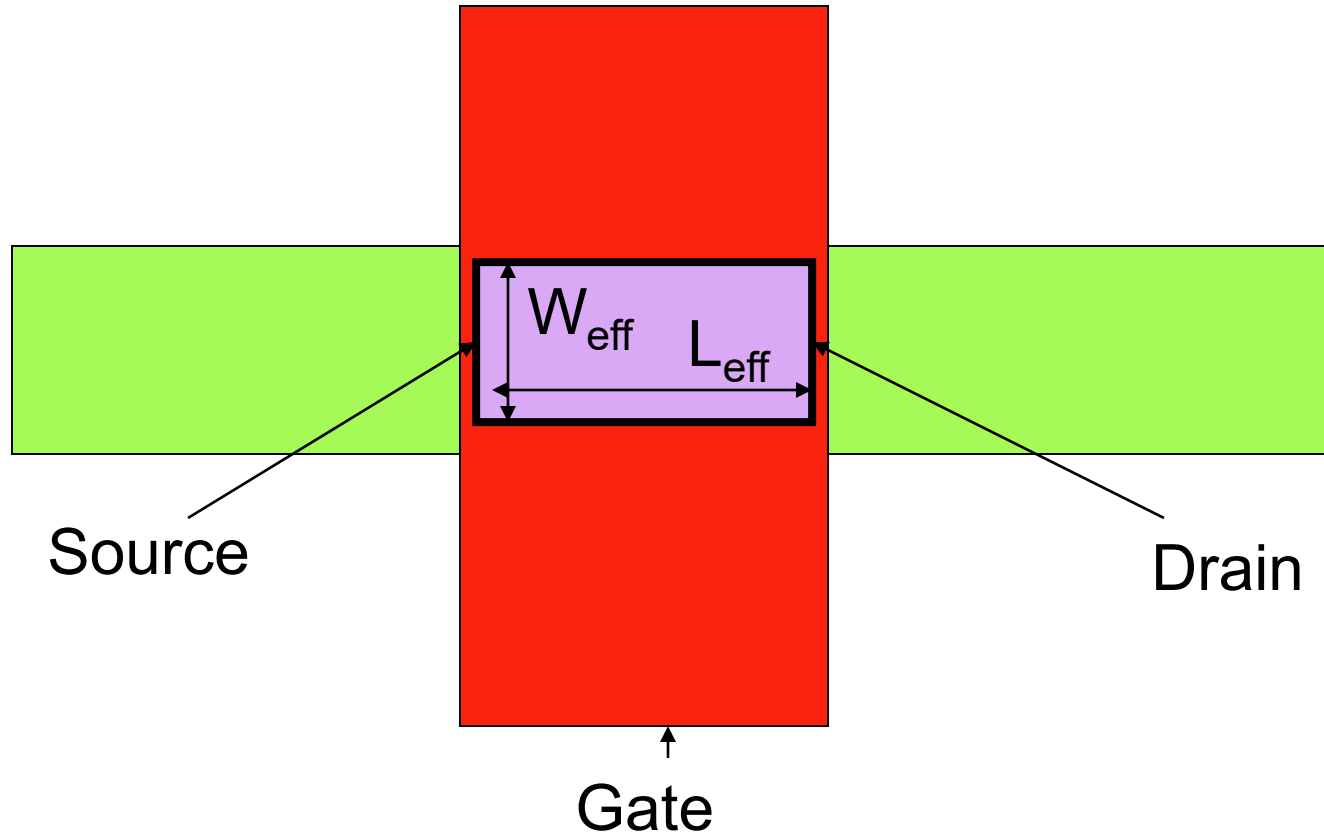
Henceforth, will assume planar devices unless specified to the contrary

# MOS Transistor



Actual Drain and Source at Edges of Channel

# MOS Transistor



Effective Width and Length Generally  
Smaller than Drawn Width and Length



Stay Safe and Stay Healthy !

**End of Lecture 3**